**REMARKS/ARGUMENTS**

Claims 1-28 remain in this application. Applicant respectfully requests that the above-identified application be reconsidered in view of the following remarks.

Claims 1, 3, 5-9, 11, 13-16, 23, 25, 27 and 28 are rejected under 35 U.S.C. § 102(e) as being anticipated by McCord (US-2003/0076125). Claims 2, 4, 10, 12, 17-22, 24 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McCord (US-2003/0076125), in view of Kanda et al. (U.S. Patent 6,671,787). As requested by the Office Action, a clear version of the drawing sheet for Figure 4 is submitted herewith (see page 8 of this response).

Applicant submits that the cited references do not teach, suggest or disclose at least "[a] DDR apparatus comprising: a pattern generating device to generate a clock test pattern and a data test pattern ..." (e.g., as described in the embodiment of claim 1).

The Office Action asserts that McCord teaches the above limitations, alleging more specifically that it teaches that sequencer 100 is coupled to CPU 30 by a communication interface 102 through which sequencer 100 receives test parameters, test data, correct test results, and test procedures, which are stored by sequencer 100 in random access memory (RAM) 104. It further alleges McCord also teaches sequencer 100 is further connected to a DDR memory controller 236, which controls DUT 14 through relays 92 and connector 22.

Applicant notes that a) the Office Action does not actually cite to any sections in McCord, but rather relies on a general cite to the sequencer element 100 and b) does not actually allege the sequencer 100 of McCord *generates* clock test patterns and data test patterns as specifically recited in the embodiment of claim 1. Applicant submits the

McCord reference does not actually disclose anywhere that sequencer 100 *generates* any clock or data test patterns in its disclosure, and that for at least the following reasons it is not the equivalent of a pattern generating device *used to generate a clock test pattern and a data test pattern* (as specifically recited in the embodiment of claim 1).

In describing the operation of the sequencer 100, paragraphs [0062] and [0063] of McCord state:

> [0062] In addition to the thermal sensor 58 and thermal control logic 56 discussed above, tester logic 50 includes a sequencer 100, which may comprise, for example, a general-purpose processor, a plurality of bit-slice (e.g., 4-bit) processors working in concert, or an application-specific integrated circuit (ASIC). *Sequencer 100 is coupled to CPU 30 by a communication interface 102 through which sequencer 100 receives test parameters, test data, correct test results, and test procedures, which are stored by sequencer 100 in random access memory (RAM) 104. Sequencer 100 also receives a reset signal 36 that, when asserted by CPU 30, causes sequencer 100 to reset itself to a known stable state by reference to configuration parameters stored within non-volatile random access memory (NVRAM) 106.* The operation of sequencer 100 is timed by a clock 108, which may be asynchronous the clocks utilized to operate DUT 14.
>
> [0063] Sequencer 100 is further connected to a DDR memory controller 236, which controls DUT 14 through relays 92 and connector 22. The depicted arrangement of sequencer 100, DDR memory controller 236, connector 22 and DUT 114 simulates the memory subsystem of a personal computer system or other end-use environment of DUT 14. *That is, sequencer 100, much like the CPU of a computer system, issues commands and requests to DDR memory controller 236, which can be implemented as a conventional complementary metal-oxide-semiconductor (CMOS) memory controller.* Memory controller 236, in turn....*(emphasis added)*

First, Paragraph [0062] discloses that the sequencer may be a general purpose *processor or group of processors.* It further states that the sequencer is coupled to a CPU by a communication interface by which sequencer 100 *receives* test parameters, test data, correct test results, and test procedures, and stores such data. Therefore, the sequencer 100 does not actually *generate test patterns* at all, but rather acts merely as a store for test results and test procedures. Storing test results and procedures is not the equivalent of generating test patterns.

McCord goes on to disclose that the sequencer 100 of McCord resets itself to a stable state upon receiving instruction from CPU 30, a functionality completely unrelated to test pattern generation. Similarly Paragraph [0063] fails to disclose the relevant limitations as well. Initially, paragraph [0063] describes the elements such as memory controllers, relays and connectors that the sequencer is connected to. The paragraph then asserts that the purpose of the sequencer 100 is, to issue commands and requests to the DDR memory controller 236, *not unlike a traditional CPU.* Test pattern generation is not a traditional purpose or capability of a CPU.

These sections do not disclose sequencer's ability to "...to generate a clock test pattern and a data test pattern ..." (as specifically recited in the embodiment of claim 1). Moreover, the McCord does not disclose that the sequencer 100 has such a capability anywhere in its disclosure. Therefore, Applicant submits that the sequencer 100 is inadequate to serve as the basis of a proper §102(e) reference, and in order to be a proper §102(e) reference, the cited reference must disclose a *pattern generating device* to generate a clock test pattern and a data test pattern, as found, for example, in the embodiment of claim 1.

Applicant further submits that the Kanda reference fails to make up for the deficiencies of McCord. Although Kanda is directed towards semiconductor memory device testing, the reference fails to disclose pattern testing, clock test patterns and data test patterns altogether.

Therefore, since the cited references fail to disclose at least a pattern generating device to generate a clock test pattern and a data test pattern, it is inadequate to support a proper §102(e) rejection. Independent claims 9, 17, 23 contain similar allowable limitations as well. Claims 2-8, 10-16, 18-22 and 24-28 are allowable for depending

from allowable base claims, and the §103(a) rejection should be withdrawn as well.

For all the above reasons, the Applicant respectfully submits that this application is now in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: October 20, 2005

By: _____
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## AMENDMENT TO THE DRAWINGS

The attached sheet of drawings includes changes to Fig.1-4. Replacement sheets 1-4 are submitted to replace any previous versions. Annotated Sheets showing changes are included as well.

Attachment: Replacement Sheets
Annotated Sheet Showing Changes

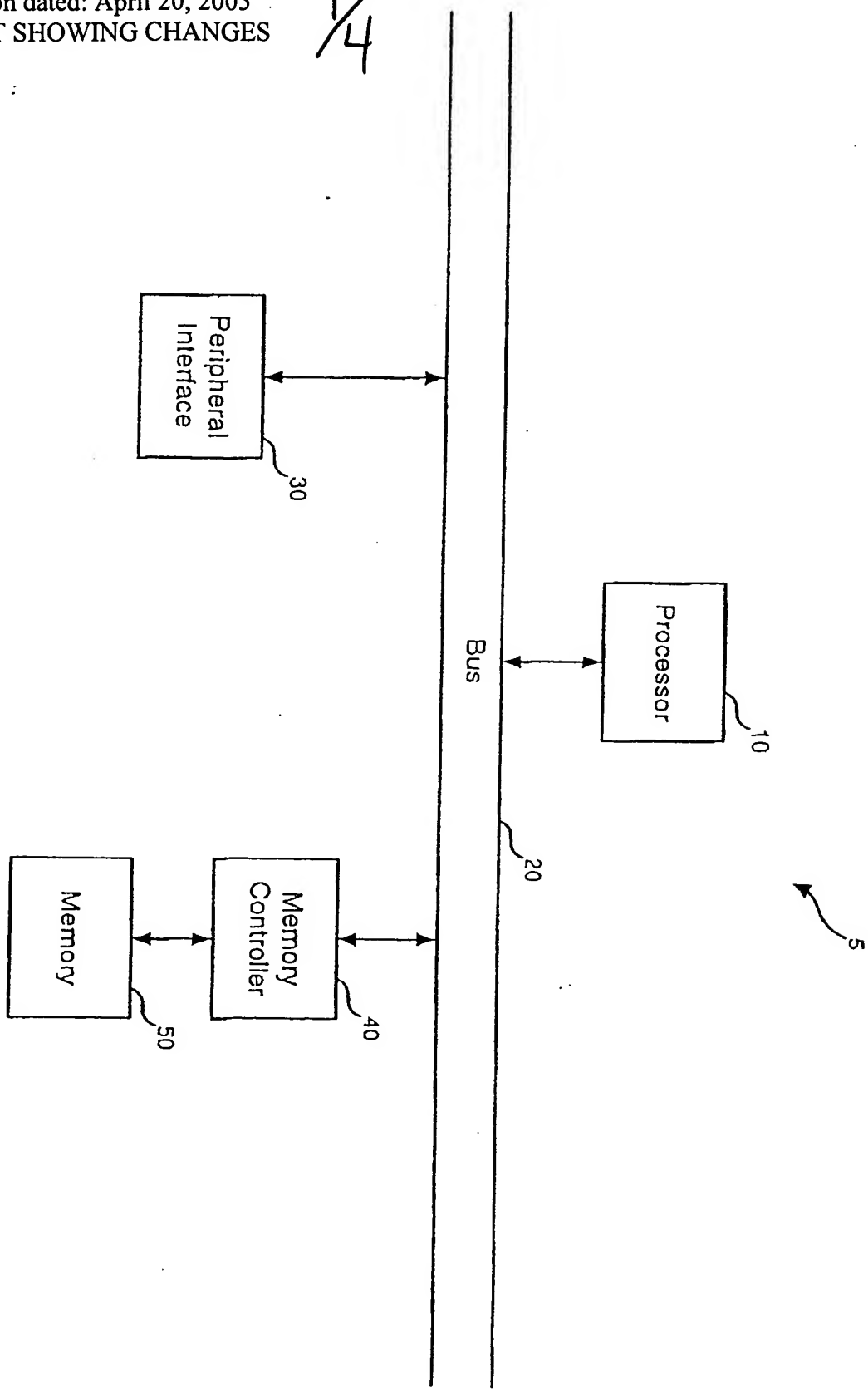
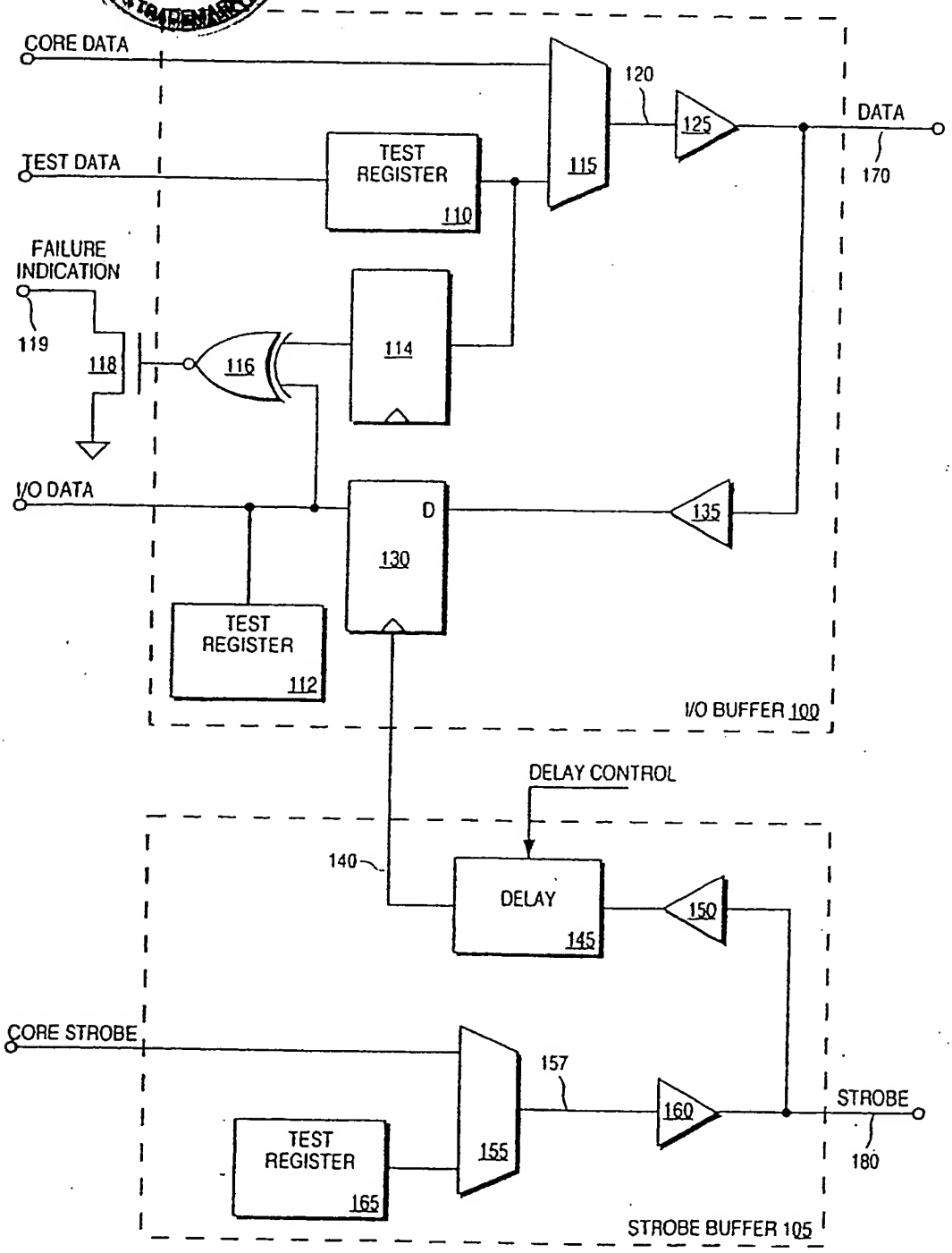


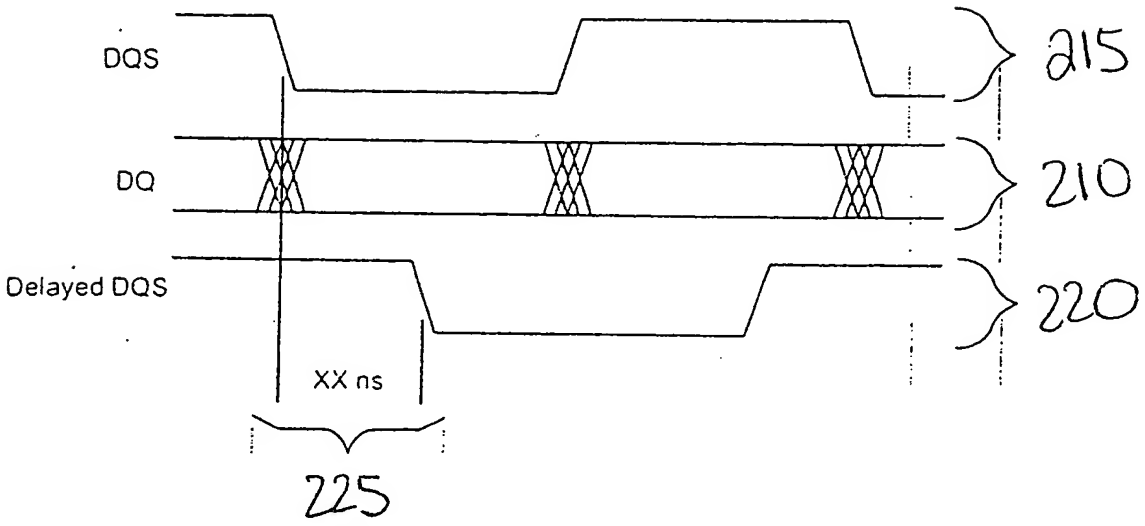

FIG. 1

Figure 1

Application No.: 10/025,760
Amendment dated: October 20, 2005
Reply to Office Action dated: April 20, 2005
ANNOTATED SHEET SHOWING CHANGES




~~FIG. 2~~ Figure 2




~~FIG 3~~

Figure 3

Application No.: 10/025,760
Amendment dated: October 20, 2005
Reply to Office Action dated: April 20, 2005
ANNOTATED SHEET SHOWING CHANGES

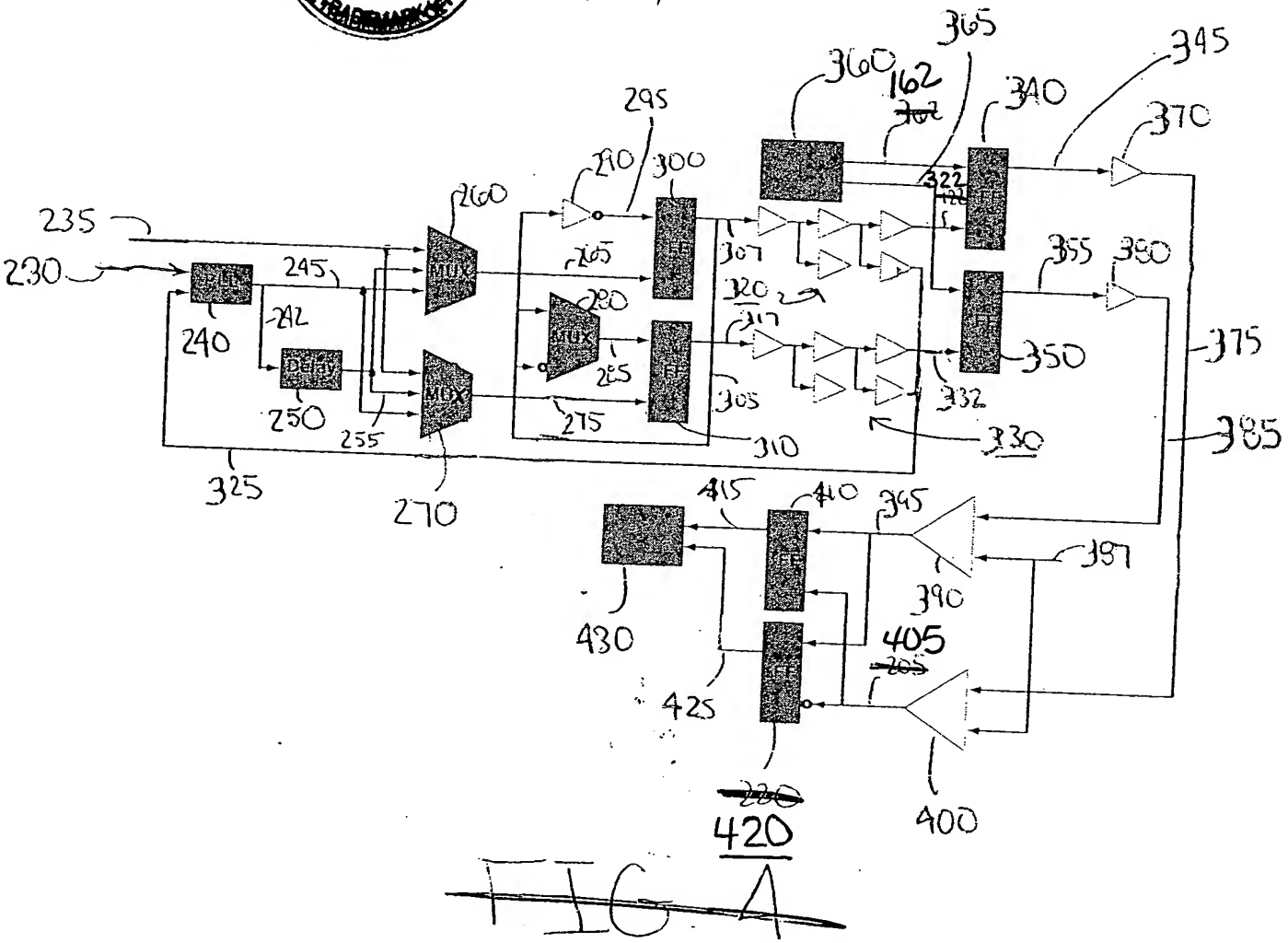



FIG 4

Figure 4